AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

A dedicated front-end for readout of strip detectors in the LHCb Upgrade experiment

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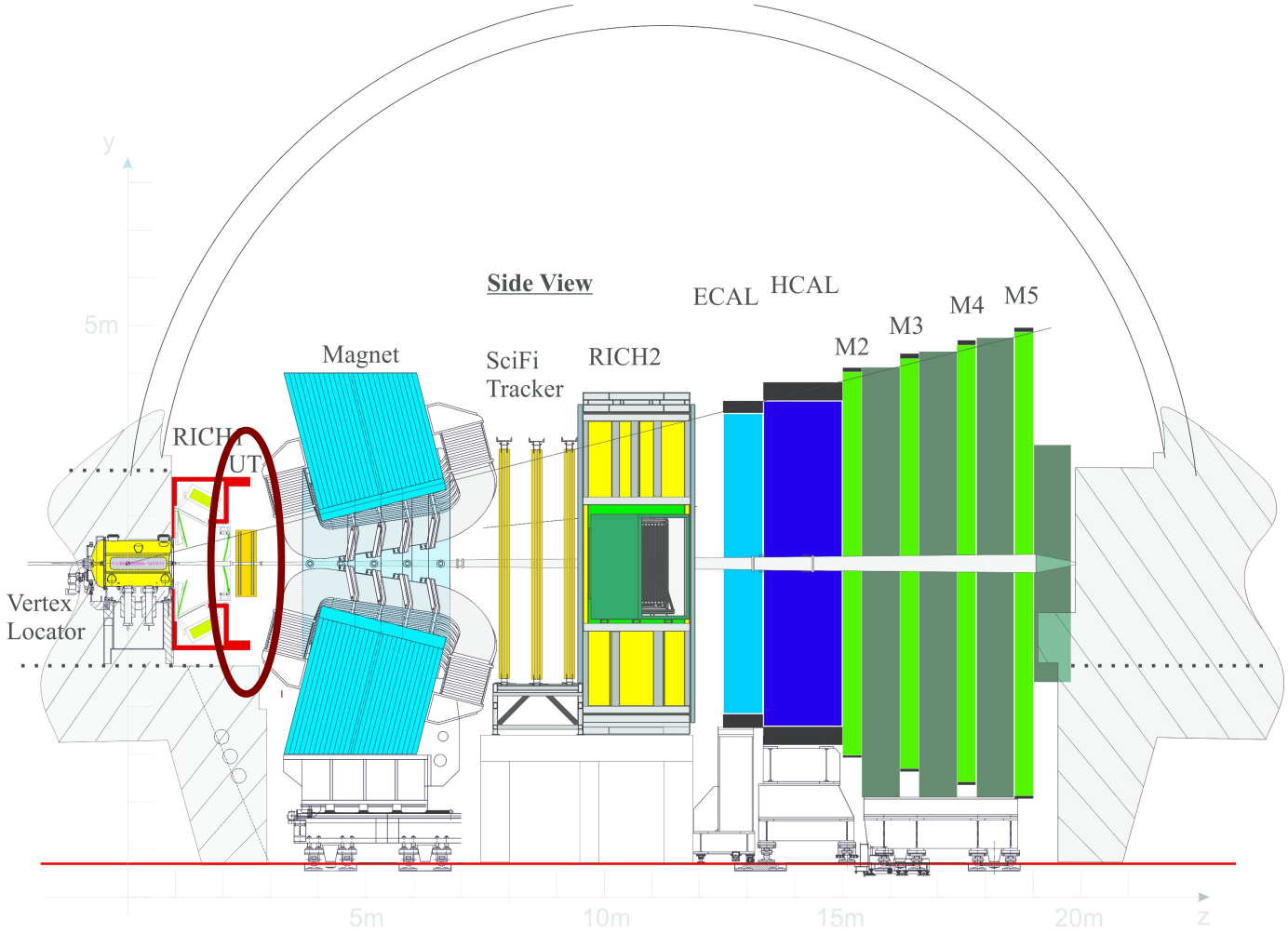
Outline

- Motivation
- SALT readout ASIC for LHCb Upstream Tracker
- Analog front-end
  - Architecture
  - Simulations
  - Measurements results
- 6-bit ADC results at a glance
- Summary

Motivation
LHCb Upgrade



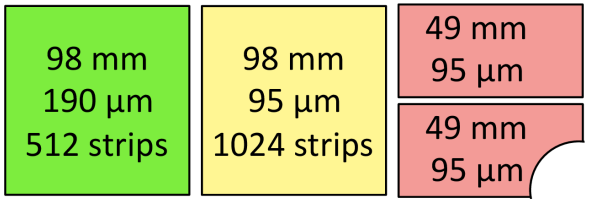
The Goal:

Replace 1 MHz Hard. trig. + Software trig. with Software trigger (40 MHz readout)

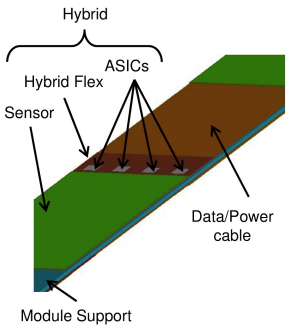
→ **new readout electronics** needed for ~0.5M silicon strip detector channels in LHCb Upstream Tracker System (present TT - Trigger Tracker)

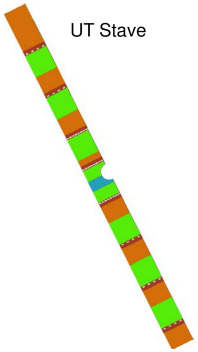
Motivation
UT – Upstream Tracker silicon strip detector

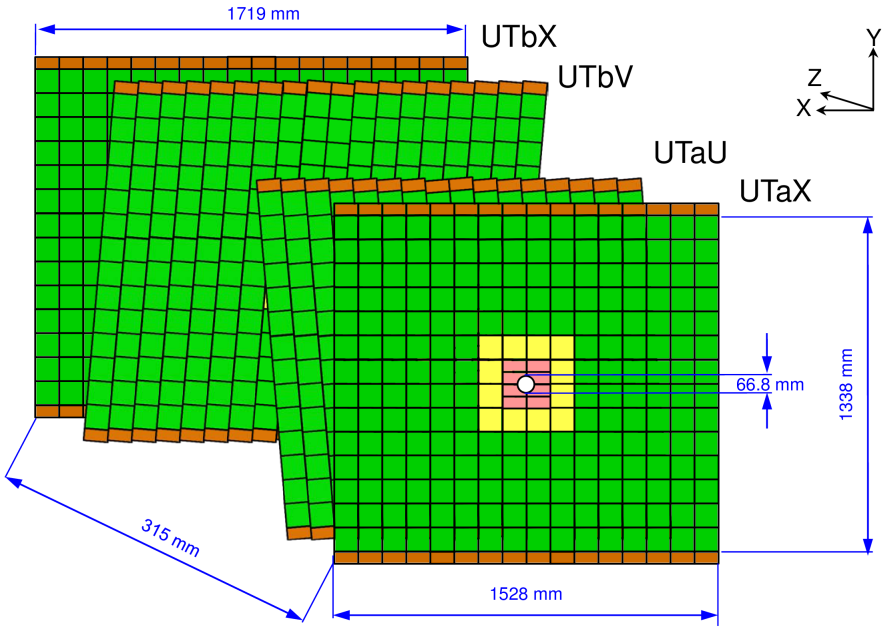
- 4 planes of silicon strip detectors
- Single sided sensors with various pitch and length



- Strips vertical on X, ±5° on U/V planes
- 68 staves, ~0.5M channels



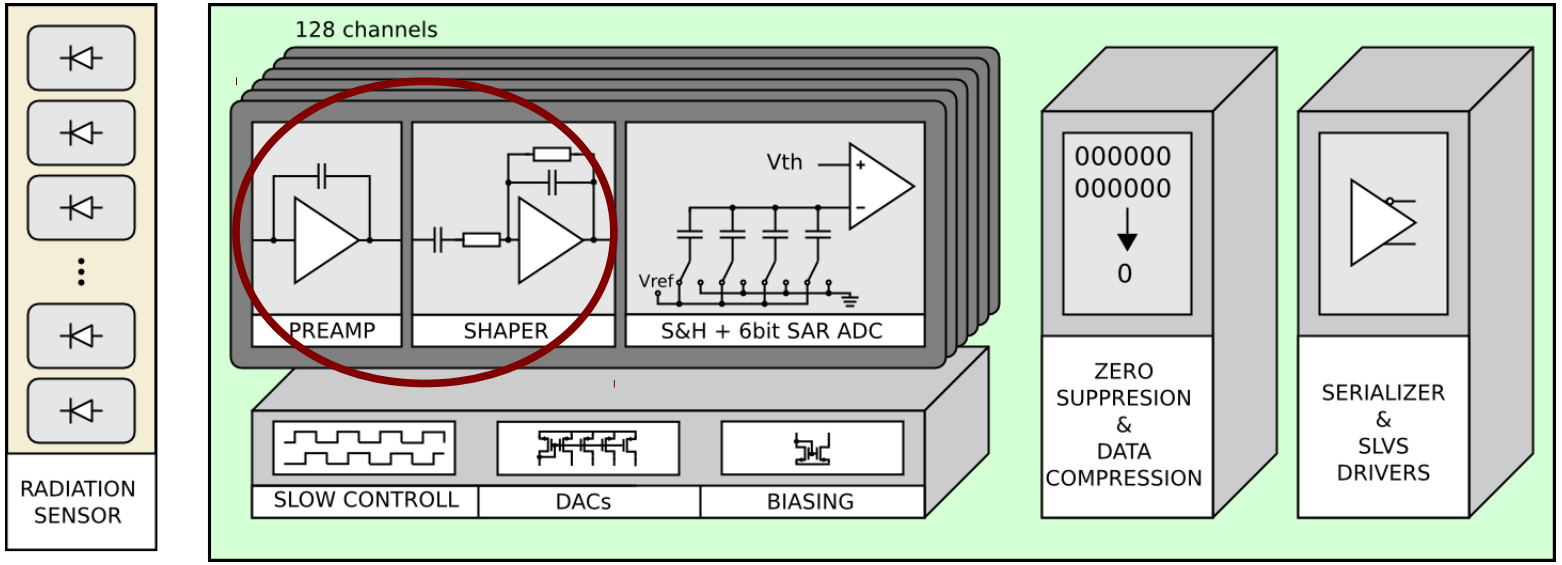




SALT – readout ASIC for UT detector Specifications

- CMOS 130 nm technology
- 128 channels, Front-end&ADC in each channel
- Pitch ~70-80 um
- Sensor: capacitance 5–20 pF, AC coupled
- Both input signal polarities (p-in-n and n-in-p sensors)
- Input charge range ~ 30ke^-
- Noise: ENC ~ 1000e^- @10pF + 50e^-/pF
- Pulse shape: T_{peak} ~25 ns, very short tail: ~5% after 2*T_{peak}
- Crosstalk < 5%
- ADC: 6-bit resolution (5-bit/polarity), 40MS/s
- DSP functions: pedestal and common mode subtraction, zero-suppression
- Serialization&Data transmission: 320 Mbps e-links to GBT, SLVS I/O
- Slow control: I2C
- Power < 6 mW/channel
- Radiation hardness ~ 30 MRad

SALT – readout ASIC for UT detector Architecture&Status

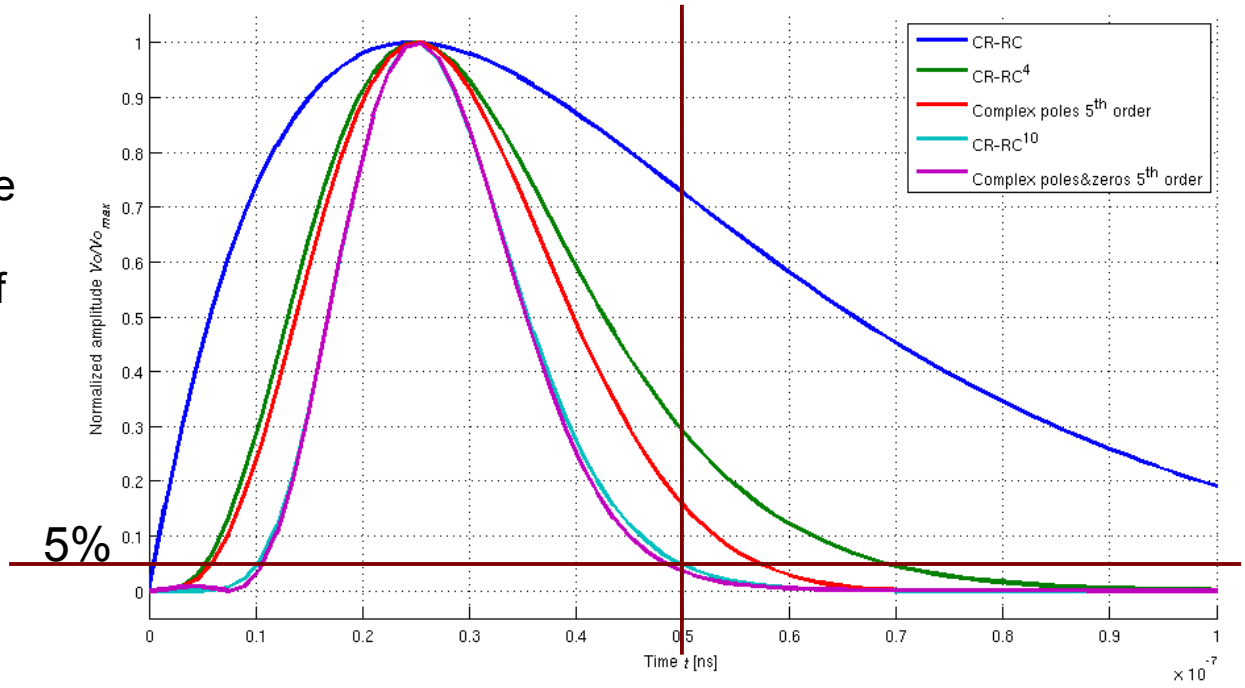


- SALT - complex SoC (System on Chip) type ASIC comprising Analog Front-end, ADC, DACs, PLL, DLL, SLVS, DSP, I2C, blocks
  - Two submissions of key prototype blocks done in 1st CMOS 130 nm process
  - Prototypes of Preamplifier&Shaper, Sampling with Single-to-Diff converter, 6-bit ADC, SLVS, PLL, DLL, designed&fabricated
  - Now we are moving to new CMOS 130 nm process
- Design and measurements of the Analog Front-end (**Preamp&Shaper**) plus short ADC status, are shown in this talk

Analog Front-end
Searching for Shaper with shortest tail

Is it possible, with realistic shaper complexity and power consumption, to shorten the pulse tail to decrease to 5% of pulse amplitude after $2*T_{peak}$?

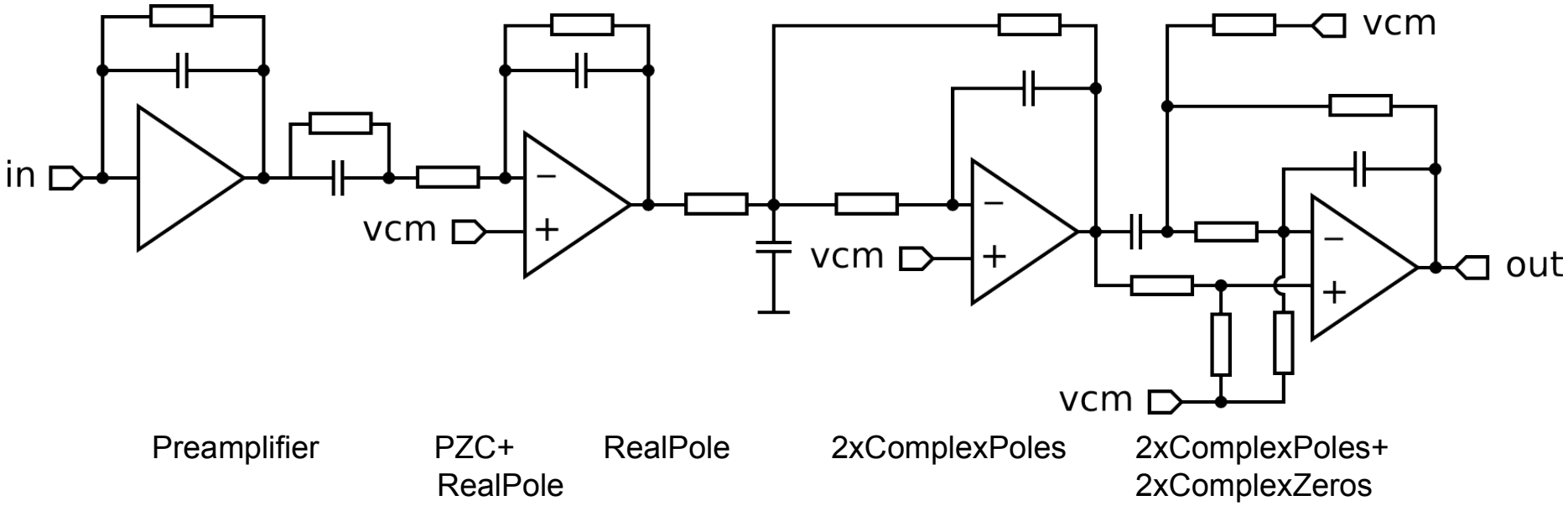
Matlab simulations of the front-end response for various configurations of poles and zeros in the shaper transfer function



Introducing complex poles and zeros in transfer function one can shorten the pulse tail to the required goal

Analog Front-end Architecture

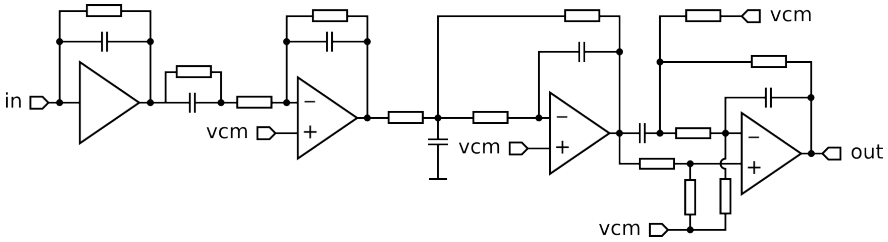
Simplified circuit diagram



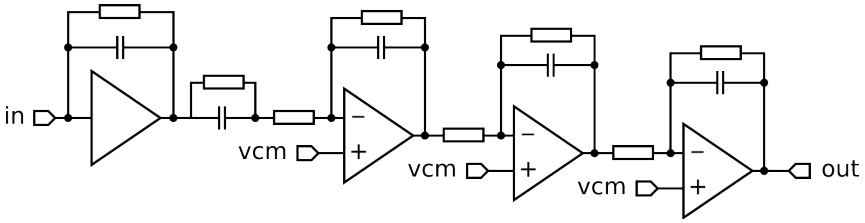
With Preamplifier + PZC and three Shaper stages (Integrator + MultipleFeedback + Boctor) the required transfer function can be obtained

Analog Front-end
Comparsion to semi-gaussian shaping

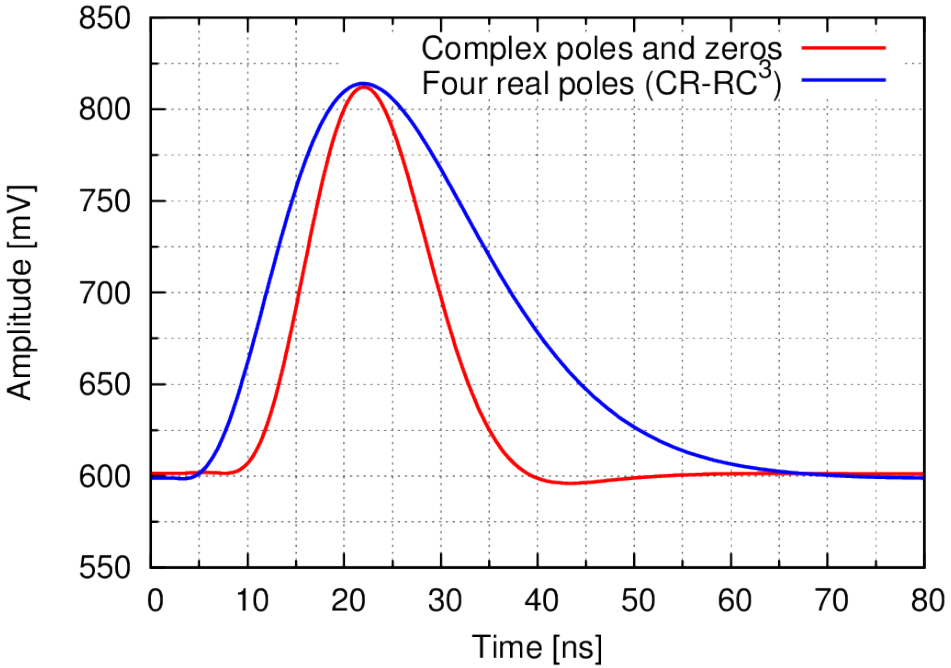
Complex poles&zeros



Four real poles (CR-RC^3)



Spectre simulations



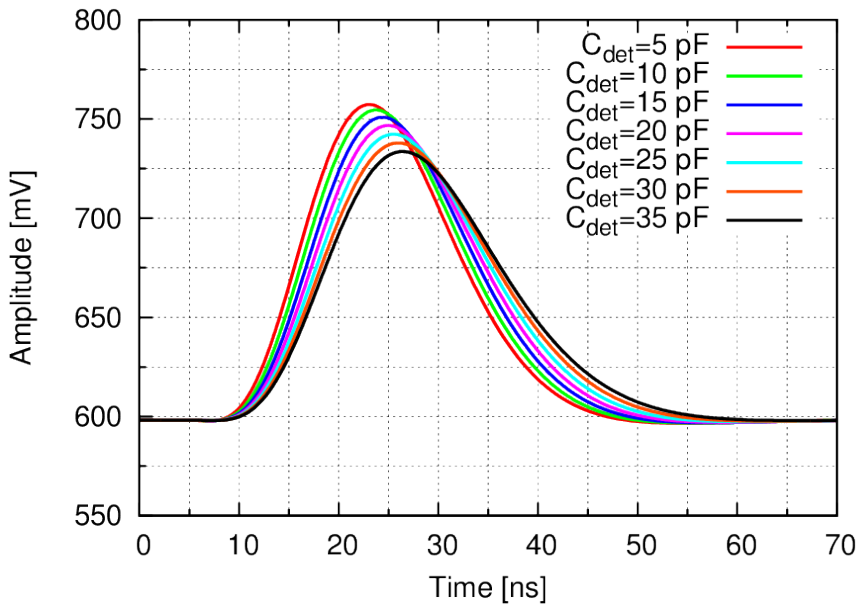
Applied shaping is much more efficient than semi-gaussian in shortening the pulse

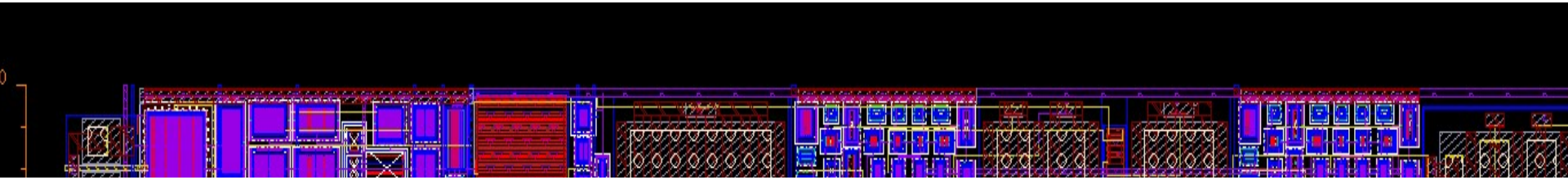
Analog Front-end Simulations, parameters

Main features:

- Architecture: Preamplifier, PZC, Shaper
- Preamplifier: NMOS input telescopic cascode with boosting amplifiers
- Shaper: 3 stages, Recycled Folded Cascode (RFC) amplifiers to limit power consumption
- T_{peak} ~25ns
- C_{det} 5–35 pF (gain and T_{peak} depend on C_{det})
- Power consumption < 1.9 mW
- 1st prototype was submitted before design completion (PSRR, baseline stabilization, ...)

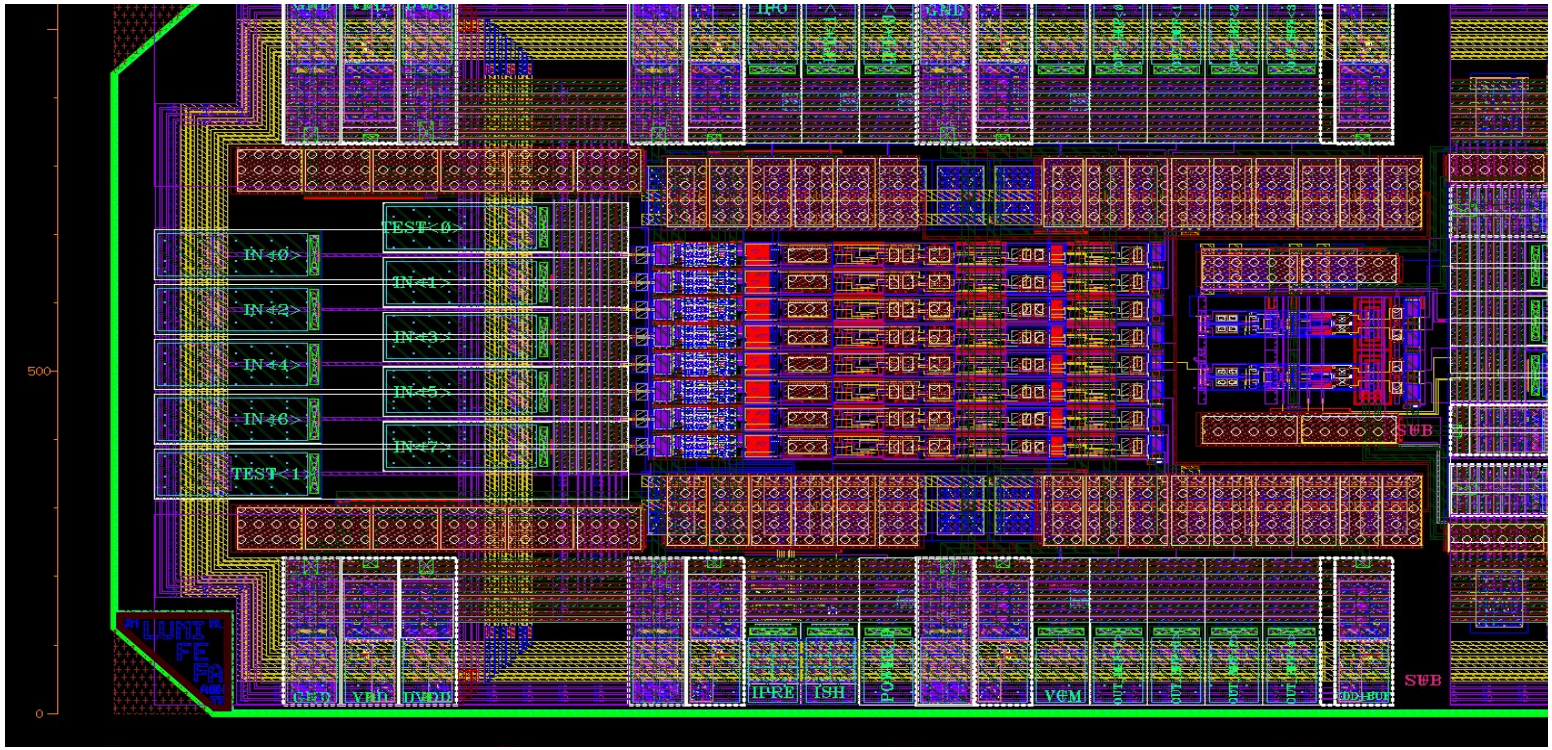
Example simulations for C_{det} 5pF – 35pF





40um x 675um , fabricated in 2013

Analog Front-end
Layout of 1st prototype

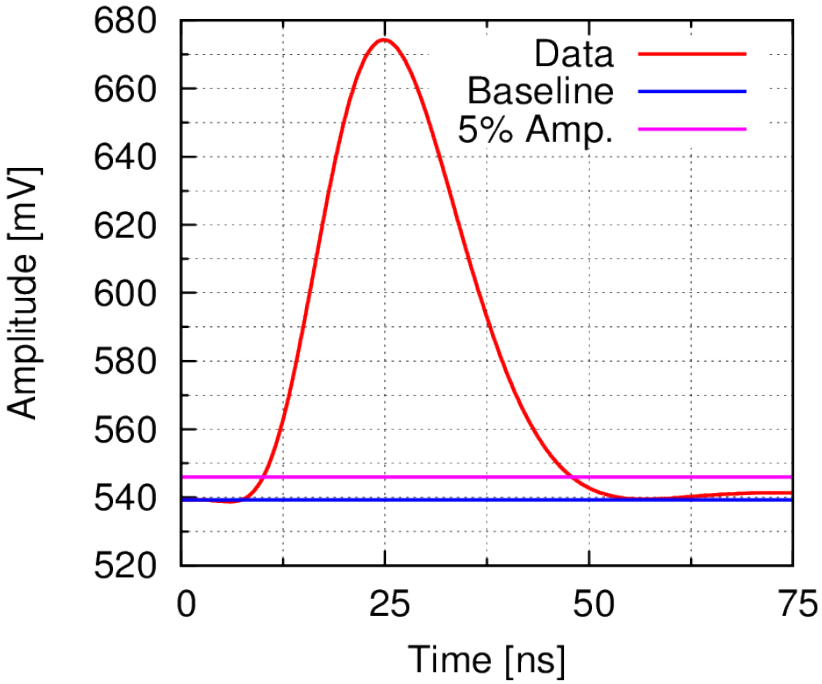


Front-end ASIC prototype contains:

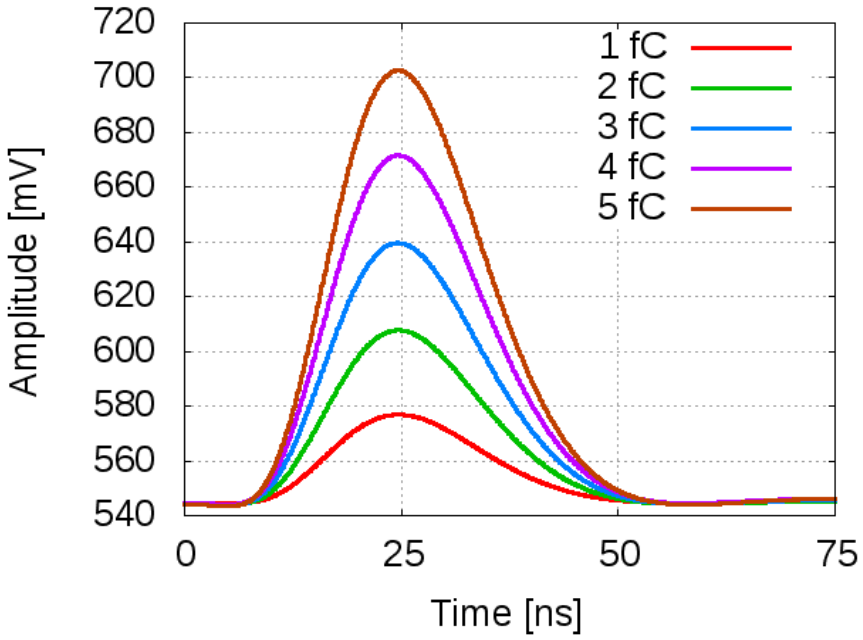
- 8 channels of Preamplifier&Shaper in pitch of 40 um
- 2 channels of Single-to-Differential converter
- Staggered pads were designed because of small channel pitch

Analog Front-end - 1st prototype
Pulse shape measurements

Example pulse response
C_{det}=10 pF, Q_{in}=4fC



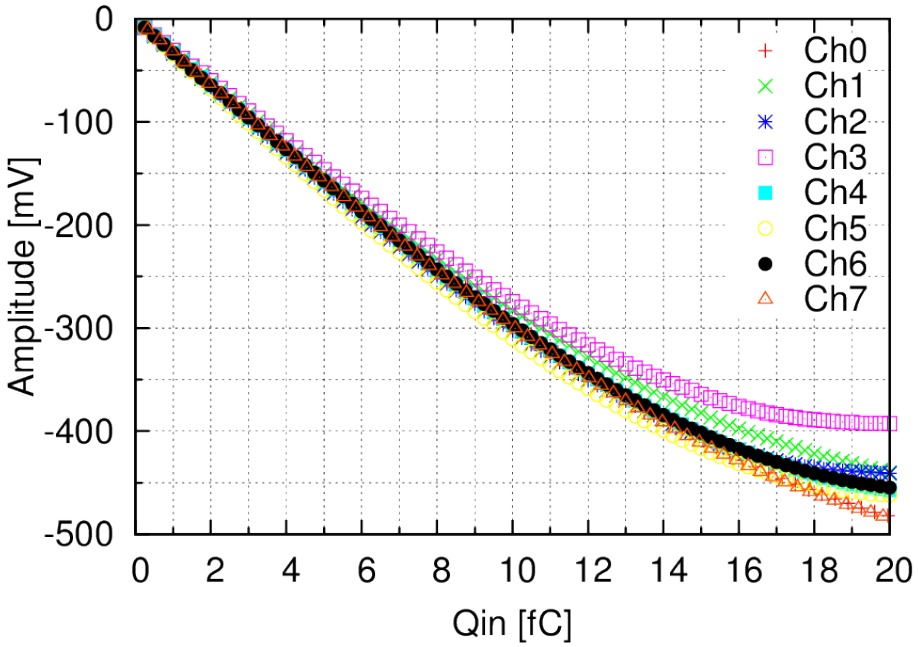
Pulses for different Q_{in}

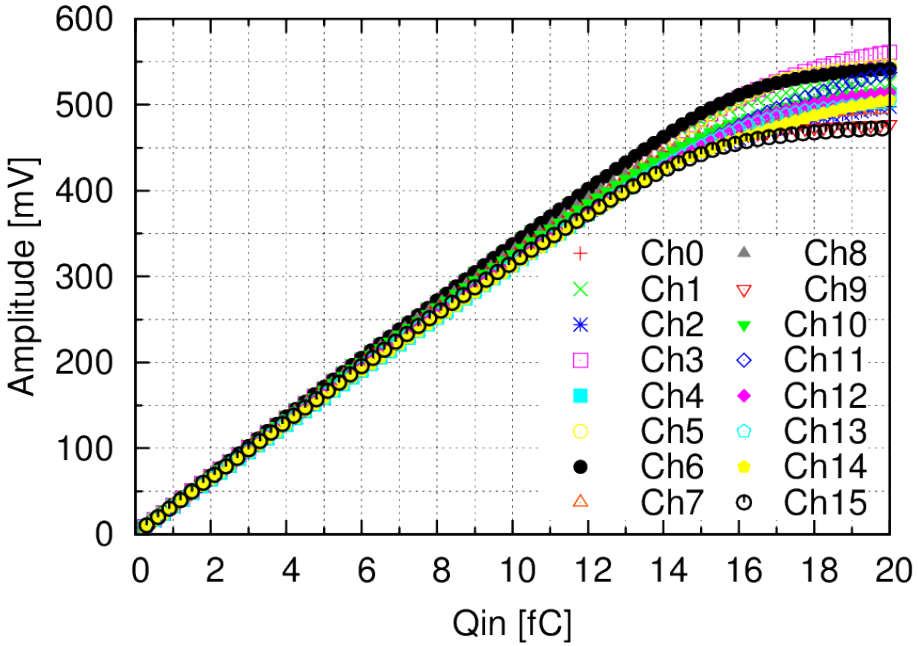


Measured shapes agree with simulations giving very short symmetrical pulses

Analog Front-end - 1st prototype Measurements of gain&linearity

Measurements of amplidute vs input charge at C_{det}=10 pF



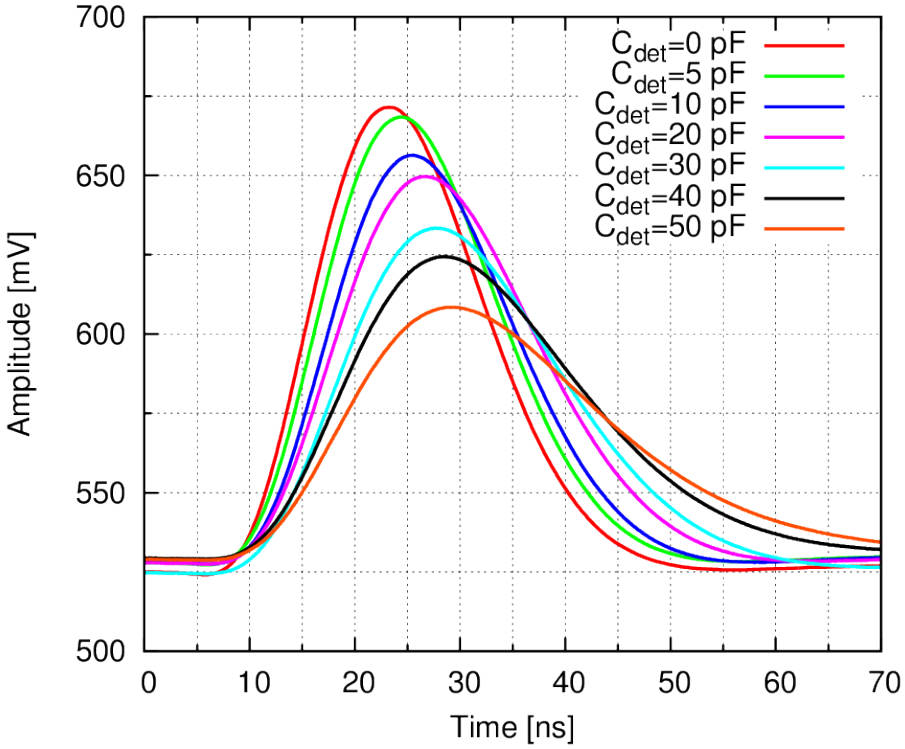


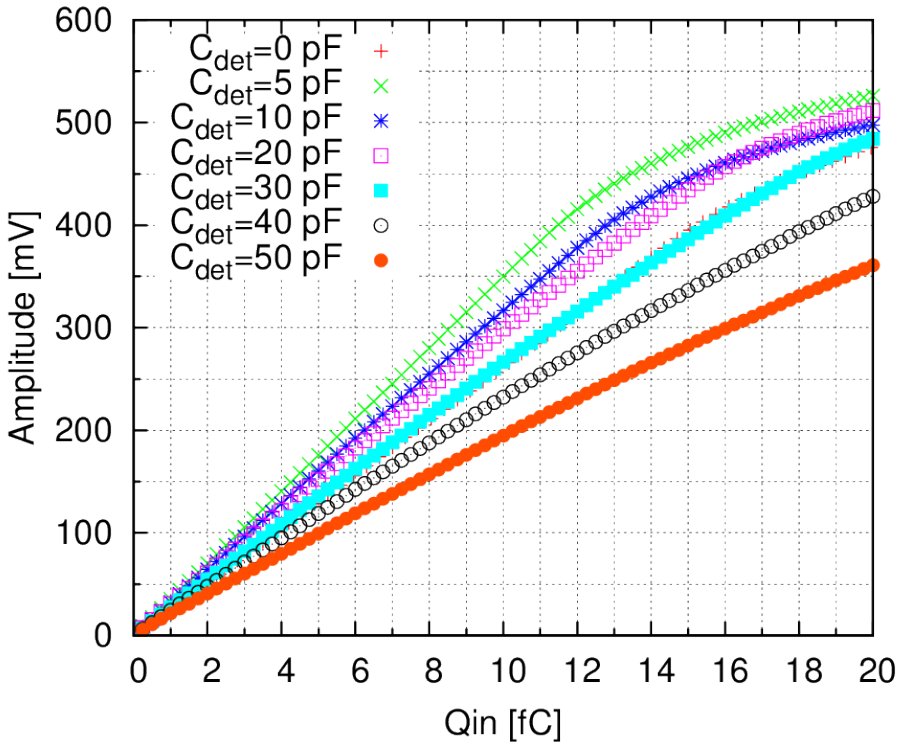
One prototype ASIC measured with negative pulses: gain is between 27.67 – 31.47 mV/fC

Two prototype ASICs measured with positive pulses: gain is between 30.13 – 32.72 mV/fC

Analog Front-end - 1st prototype
Measurements – effect of sensor capacitance

Pulse shape and gain measured for C_{det} in the range 0 – 50 pF



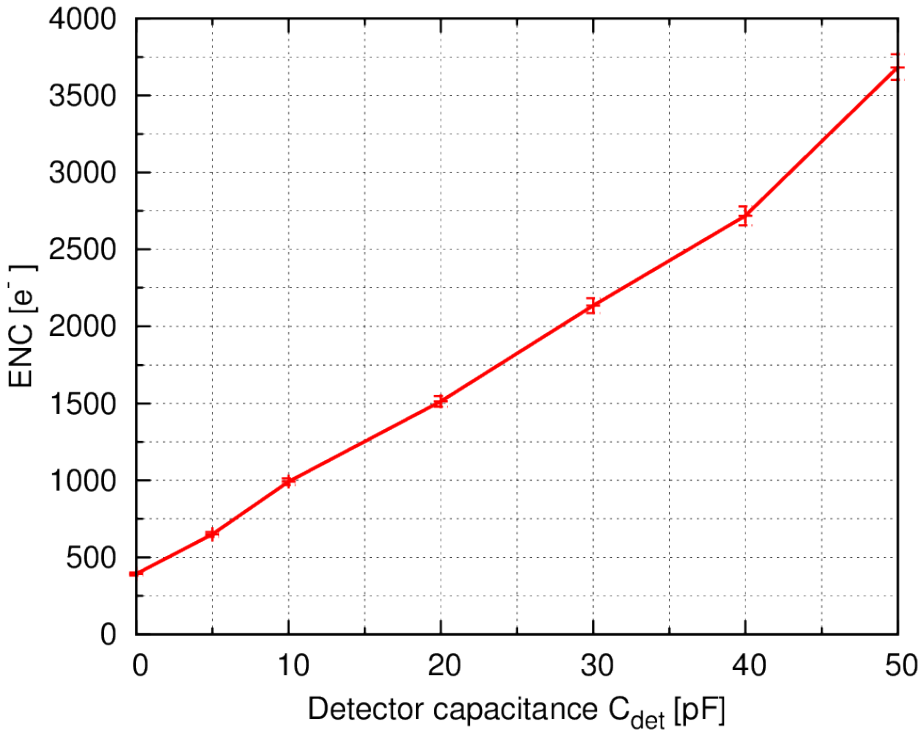


Peaking time changes from 23.5ns at 0pF to 29ns at 50pF

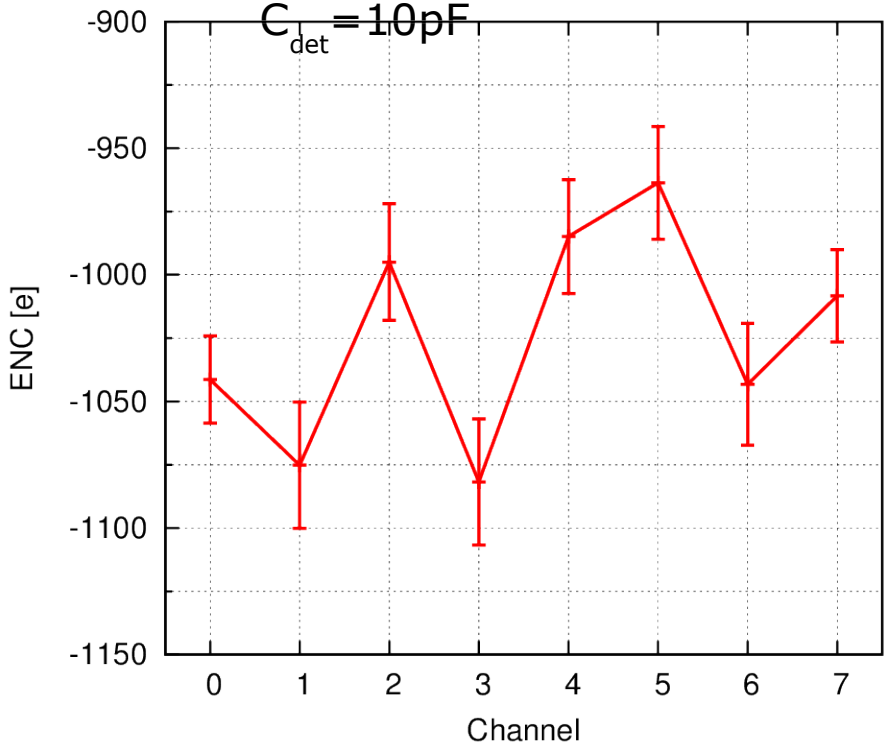
Gain changes from 36mV/fC at 0pF to 18mV/fC at 50pF

Analog Front-end - 1st prototype
Noise measurements

Measurements of noise ENC for C_{det} in the range 0pF – 50pF



ENC spread between channels for C_{det} =10pF

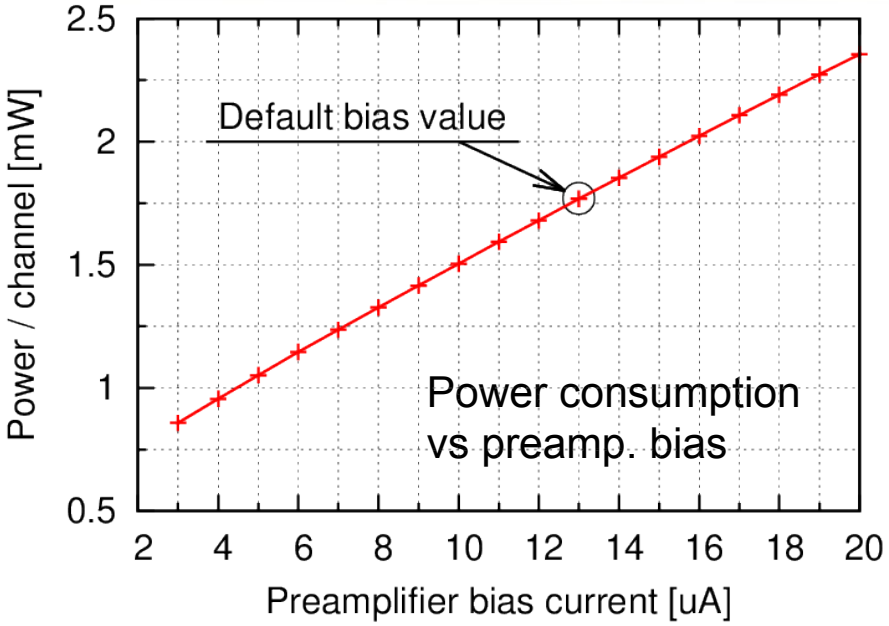


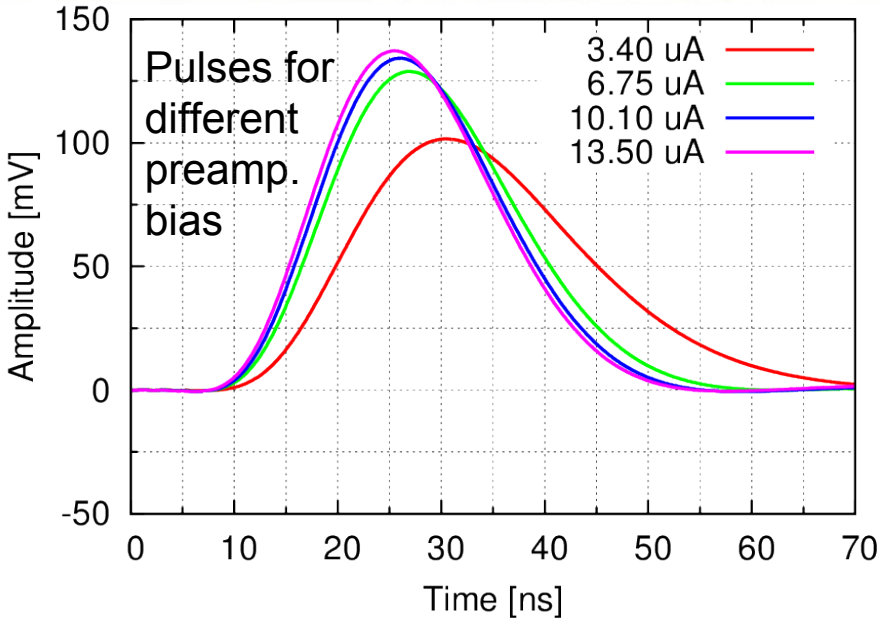
For C_{det} =10pF ENC~1000e^-

ENC slope ~57e^-/pF

Noise is uniform between the channels

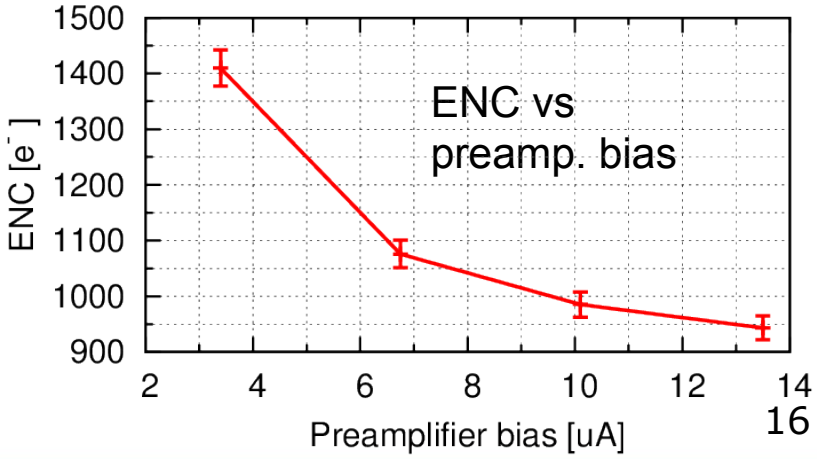
Analog Front-end - 1st prototype
Performance vs Power consumption





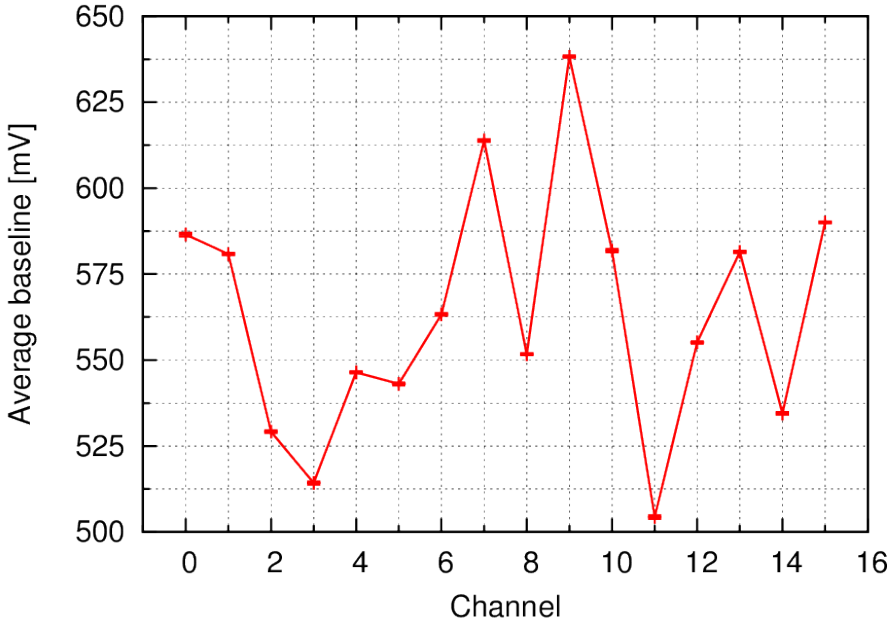
C_{det}=10 pF

Power consumption may be decreased without significant decrease of performance. Savings are also possible in shaper power consumption.

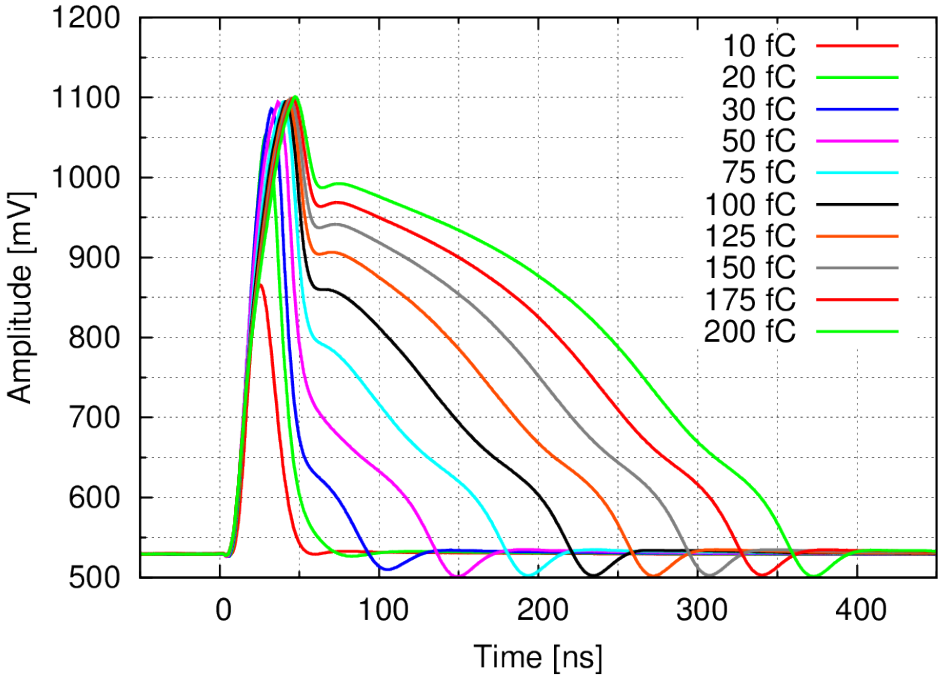


Analog Front-end - 1st prototype
Measurements of Baseline, Large Qin

Baseline spread between the channels



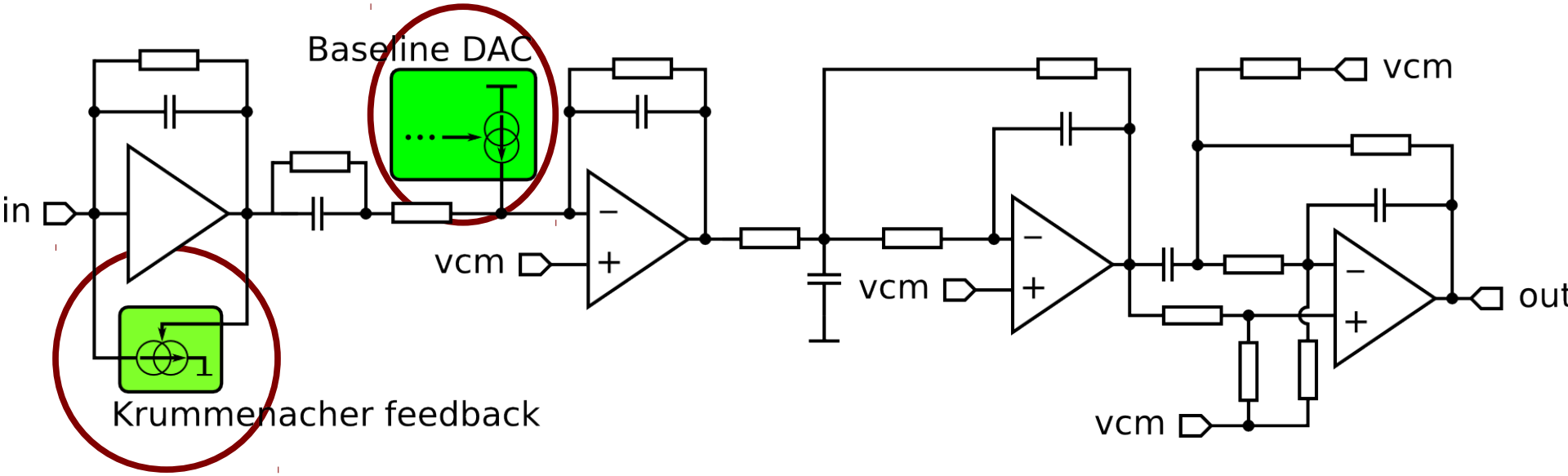
Pulse response for large Qin



Baseline spread is large (>100mV) in agreement with simulations.
A DAC will be needed to trim the baseline.

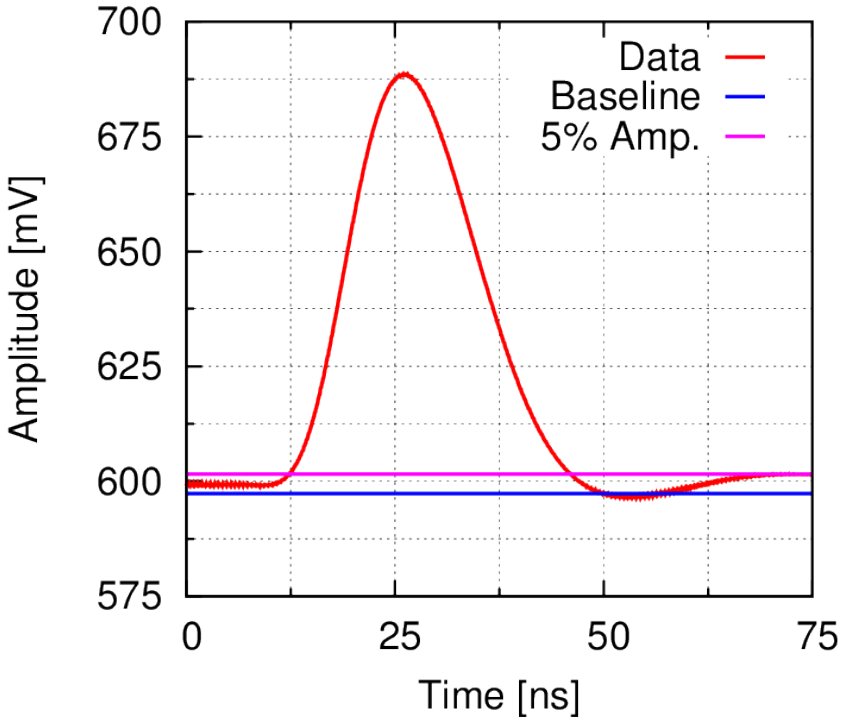
About 10-20 clock (25ns) periods are needed to recover after large charge deposition

Analog Front-end
2nd prototype architecture

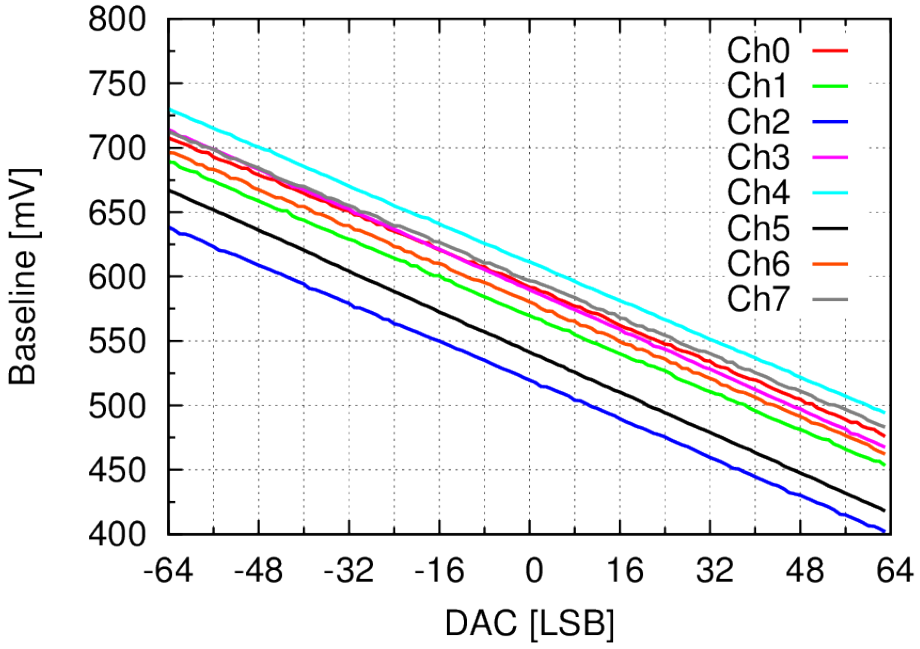


In the 2nd prototype Krummenacher type feedback was added in the preamplifier, 7-bit current DAC was added to set the baseline, and design was optimized for lower power consumption.

Analog Front-end – 2nd prototype
Preliminary measurements

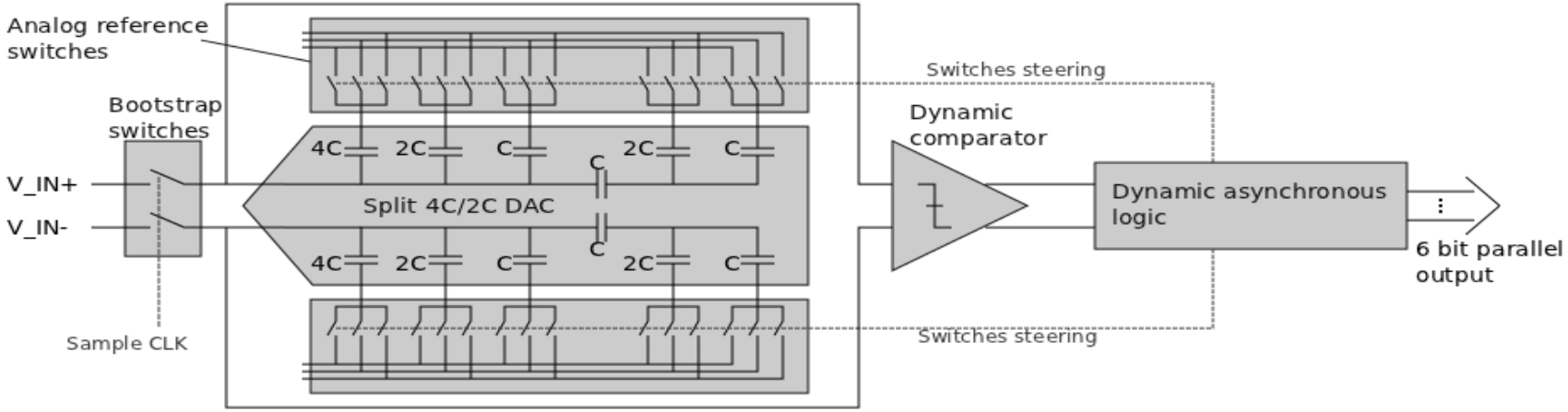


Trimming the baselines



2nd prototype works, pulses are seen, baselines may be set, power consumption is ~1mW/channel
Measurements have just started...

6-bit SAR ADC
Architecture&Design considerations



Architecture of 6-bit ADC

- Differential segmented/split DAC with MCS switching scheme – ***ultra low power***
- Dynamic comparator – ***no static power consumption, power pulsing for free***
- Asynchronous logic – no clock tree – ***power saving, allows asynchronous sampling***
- Dynamic SAR logic – ***much faster than conventional static logic***

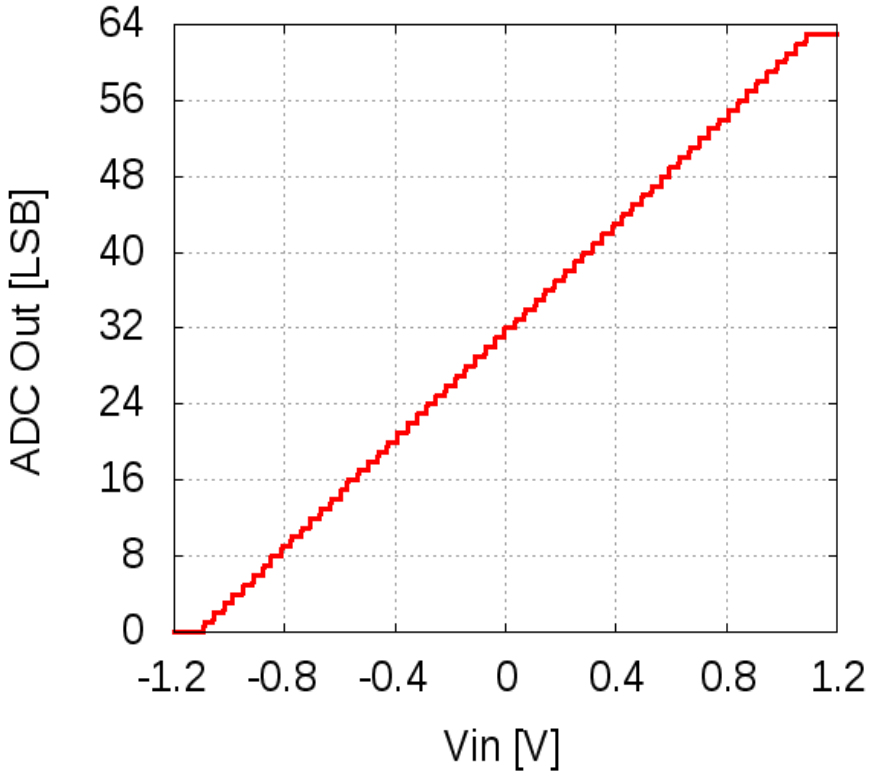
Design consideration:

- Variable sampling frequency (up to >80 MS/s) and power consumption
- Power consumption ~0.3 mW at 40 MS/s
- 40 µm pitch, ready for multichannel integration

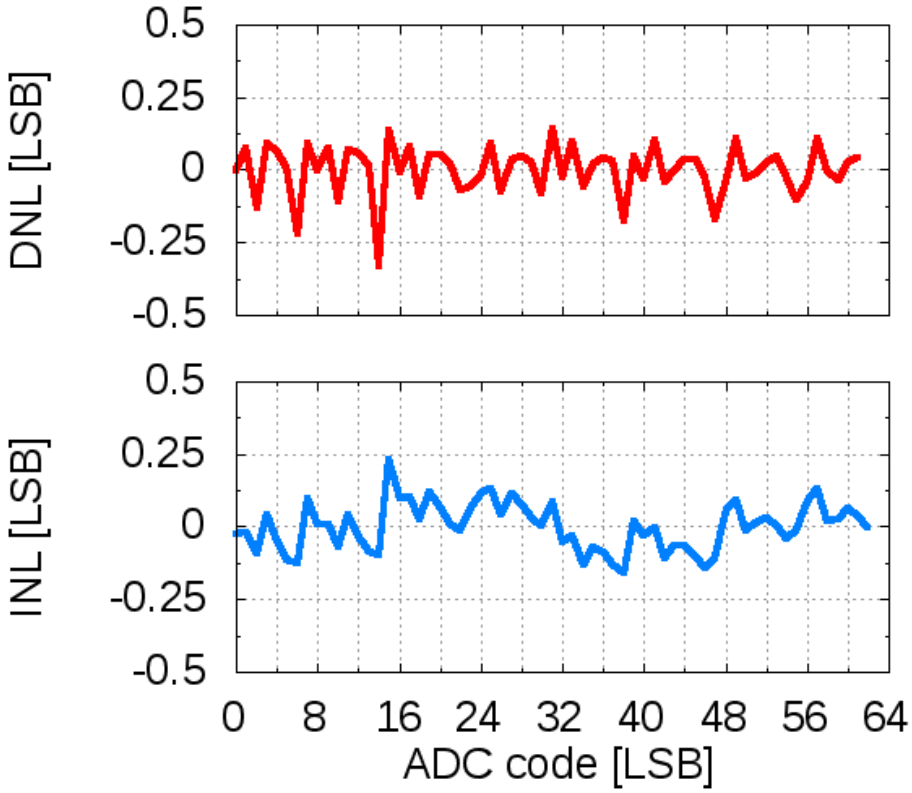
M. Firlej, T. Fiutowski, M. Idzik, J. Moroń,K. Świentek, "A fast, low-power, 6-bit SAR ADC for readout of strip detectors in the LHCb Upgrade experiment", Journal of Instrumentation, JINST 9 P07006, July 2014

6-bit SAR ADC
Static tests – linearity (@50 MS/s)

Transfer function



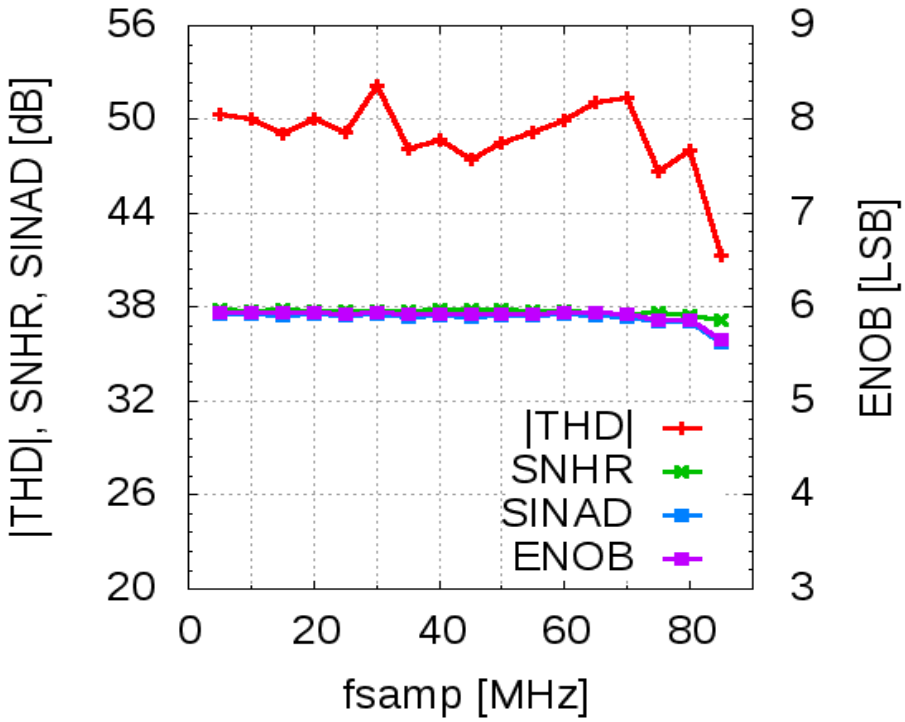
INL/DNL measurements



- Measurements show that ADC works very well
- At 50MHz sampling frequency good linearity INL, DNL < 0.4 is seen

6-bit SAR ADC
Dynamic tests, ENOB, power

Sampling frequency sweep



Main features

Resolution	**6**
Sampling frequency [Ms/s]	**>80**
Power cons. [mW] @40Ms/s	**0.35**
Size [mm^2]	**0.016**
[um x um]	**40 x 400**
DNL/INL [LSB]	**<0.4**
SINAD@40MS/s[dB]	**37.5**
ENOB[bits]	**5.8**
FOM [fJ/conv]	**~150**

Performance of our ADC is similar to State-of-the-Art designs

Summary&Plans

- Development of SALT Front-end ASIC for LHCb Upstream Tracker is on the way
  - Prototypes of key blocks (analog front-end, ADC, PLL, SLVS, …) developed in 130 nm CMOS and working
- Analog front-end architecture with symmetrical very short pulses, working for different C_{det}, low power, positively verified in lab. tests
- Design of single blocks and multichannel SALT prototype has been started in new 130 nm CMOS
- Submission of small 8-channel SALT prototype planned in 2014
- Submission of 128-channel SALT version planned in 2015

Thank you for attention